# 74HCT157

# Quad 2-Input Data Selectors / Multiplexers

## High−Performance Silicon−Gate CMOS

The 74HCT157 is identical in pinout to the LS157. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device routes 2 nibbles (A or B) to a single port (Y) as determined by the Select input. The data is presented at the outputs in noninverted form. A high level on the Output Enable input sets all four Y outputs to a low level.

### Features

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS−Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 82 FETs or 20.5 Equivalent Gates
- These are Pb−Free Devices

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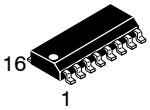
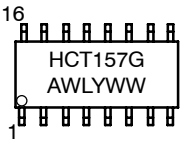
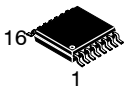
**MARKING DIAGRAMS**

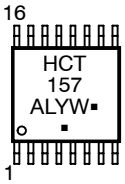



**SOIC−16**
**D SUFFIX**
**CASE 751B**




**TSSOP−16**
**DT SUFFIX**
**CASE 948F**




| | |
|---|---|
| 74HCT157 | = Device Code |
| A | = Assembly Location |
| L, WL | = Wafer Lot |
| Y | = Year |
| W, WW | = Work Week |
| G or ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

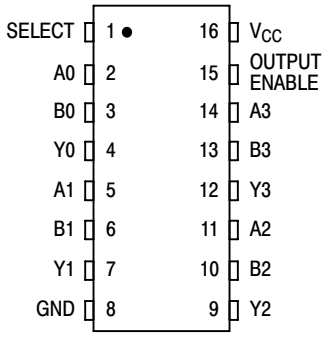



**Figure 1. Pin Assignment**

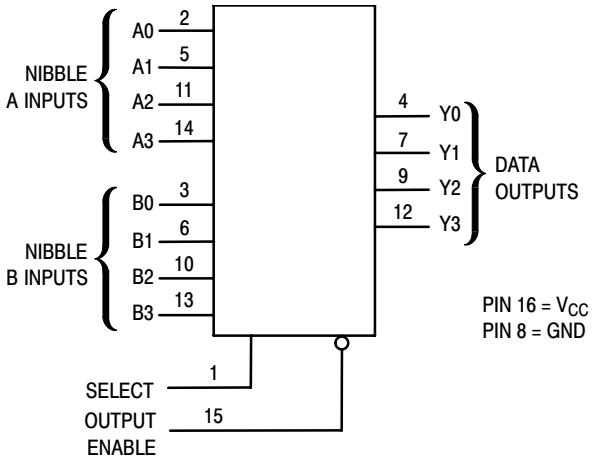



**Figure 2. Logic Diagram**

**FUNCTION TABLE**

| Inputs | | Outputs |
|---|---|---|
| **Output Enable** | **Select** | **Y0 – Y3** |
| H | X | L |
| L | L | A0 – A3 |
| L | H | B0 – B3 |

X = don't care
A0 – A3, B0 – B3 = the levels of the respective Data–Word Inputs.

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| 74HCT157DR2G | SOIC–16 (Pb–Free) | 2500 Units / Reel |
| 74HCT157DTR2G | TSSOP–16* | 2500 Units / Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb–Free.

## MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | − 0.5 to + 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | − 0.5 to $V_{CC}$ + 0.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | − 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ±20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±50 | mA |
| $P_D$ | Power Dissipation in Still Air, SOIC Package†<br>TSSOP Package† | 500<br>450 | mW |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package) | 260 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Package: − 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | | 4.5 | 5.5 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | | − 55 | + 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) | $V_{CC}$ = 2.0 V<br>$V_{CC}$ = 4.5 V<br>$V_{CC}$ = 6.0 V | 0<br>0<br>0 | 1000<br>500<br>400 | ns |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | $V_{CC}$ (V) | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | −55 to 25°C | ≤85°C | ≤125°C | |
| $V_{IH}$ | Minimum High−Level Input Voltage | $V_{out}$ = 0.1V<br>$\|I_{out}\|$ ≤ 20μA | 4.5<br>5.5 | 2.0<br>2.0 | 2.0<br>2.0 | 2.0<br>2.0 | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | $V_{out}$ = $V_{CC}$ − 0.1V<br>$\|I_{out}\|$ ≤ 20μA | 4.5<br>5.5 | 0.8<br>0.8 | 0.8<br>0.8 | 0.8<br>0.8 | V |
| $V_{OH}$ | Minimum High−Level Output Voltage | $V_{in}$ = $V_{IL}$<br>$\|I_{out}\|$ ≤ 20μA | 4.5<br>5.5 | 4.4<br>5.4 | 4.4<br>5.4 | 4.4<br>5.4 | V |
| | | $V_{in}$ = $V_{IL}$ $\|I_{out}\|$ ≤ 4.0mA | 4.5 | 3.98 | 3.84 | 3.70 | |
| $V_{OL}$ | Maximum Low−Level Output Voltage | $V_{in}$ = $V_{IH}$<br>$\|I_{out}\|$ ≤ 20μA | 4.5<br>5.5 | 0.1<br>0.1 | 0.1<br>0.1 | 0.1<br>0.1 | V |
| | | $V_{in}$ = $V_{IH}$ $\|I_{out}\|$ ≤ 4.0mA | 4.5 | 0.26 | 0.33 | 0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 5.5 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND<br>$I_{out}$ = 0μA | 5.5 | 4.0 | 40 | 40 | μA |

| | | | | | | |
|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Additional Quiescent Supply Current | $V_{in}$ = 2.4V, Any One Input<br>$V_{in}$ = $V_{CC}$ or GND, Other Inputs<br>$I_{out}$ = 0μA | 5.5 | ≥ −55°C<br>2.9 | 25 to 125°C<br>2.4 | mA |

1. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).
2. Total Supply Current = $I_{CC}$ + $\Sigma\Delta I_{CC}$.

**AC ELECTRICAL CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 6.0 ns)

| Symbol | Parameter | $V_{CC}$ (V) | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 4) | 4.5 | 21 | 26 | 32 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Select to Output Y (Figures 2 and 4) | 4.5 | 22 | 28 | 33 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 4) | 4.5 | 20 | 25 | 30 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 1 and 4) | 4.5 | 15 | 19 | 22 | ns |
| $C_{in}$ | Maximum Input Capacitance | – | 10 | 10 | 10 | pF |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Package)* | 33 | pF |

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

## PIN DESCRIPTIONS

### INPUTS

**A0, A1, A2, A3 (Pins 2, 5, 11, 14)**

Nibble A inputs. The data present on these pins is transferred to the outputs when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

**B0, B1, B2, B3 (Pins 3, 6, 10, 13)**

Nibble B inputs. The data present on these pins is transferred to the outputs when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

### OUTPUTS

**Y0, Y1, Y2, Y3 (Pins 4, 7, 9, 12)**

Data outputs. The selected input Nibble is presented at these outputs when the Output Enable input is at a low level. The data present on these pins is in its noninverted form. For the Output Enable input at a high level, the outputs are at a low level.

### CONTROL INPUTS

**Select (Pin 1)**

Nibble select. This input determines the data word to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

**Output Enable (Pin 15)**

Output Enable input. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input sets all outputs to a low level.

## SWITCHING WAVEFORMS

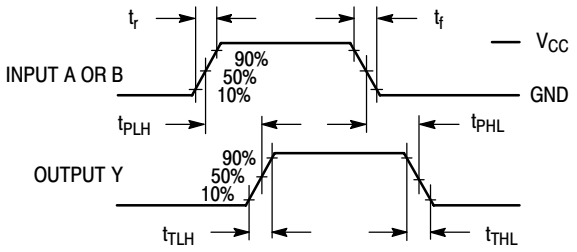



**Figure 3. HCT157**

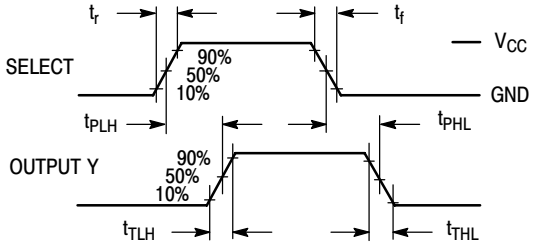



**Figure 4. Y versus Selected, Noninverted**

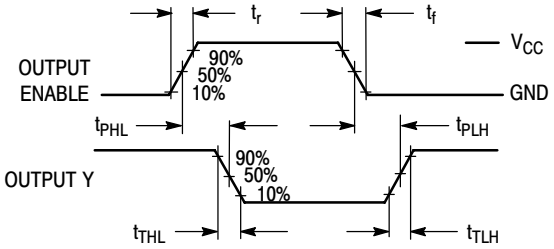
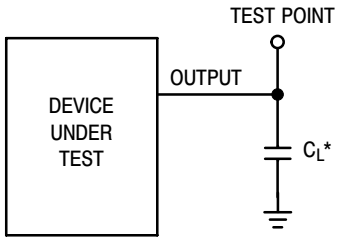


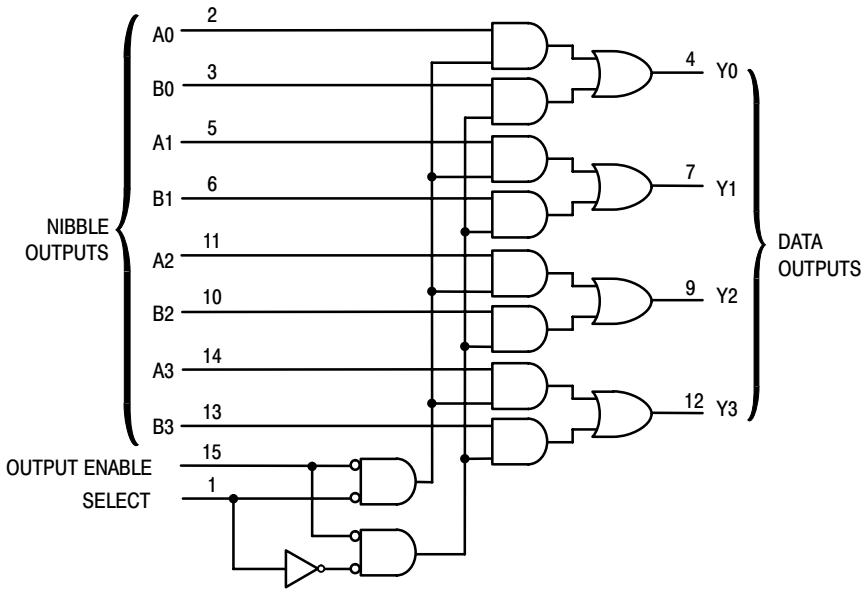

**Figure 5. HCT157**




*Includes all probe and jig capacitance

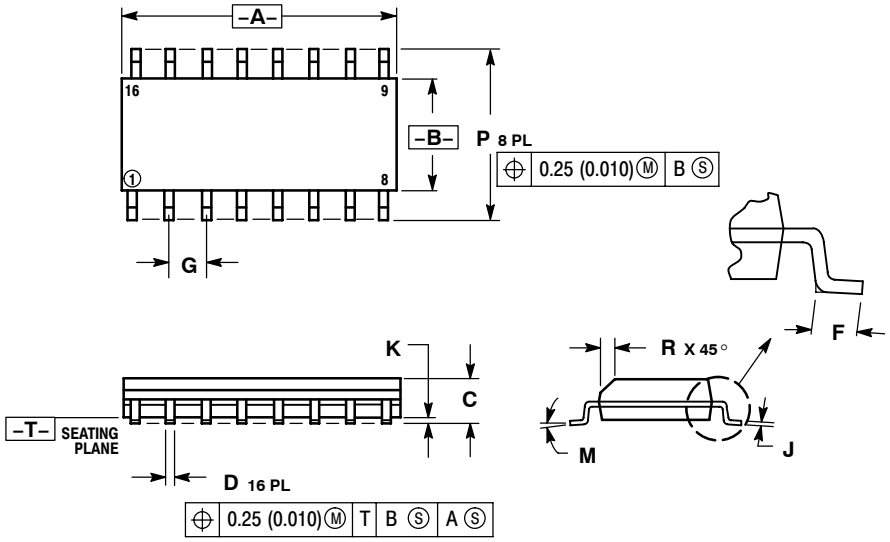
**Figure 6. Test Circuit**

## EXPANDED LOGIC DIAGRAM



## PACKAGE DIMENSIONS

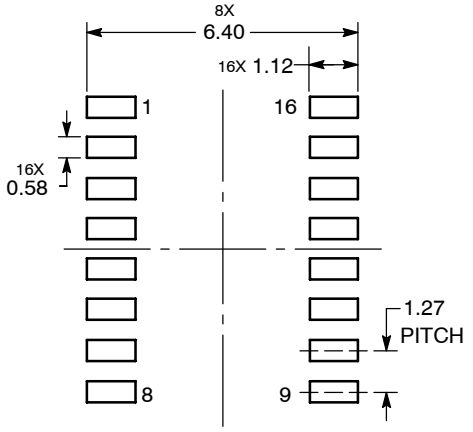
**SOIC−16**
CASE 751B−05
ISSUE K




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

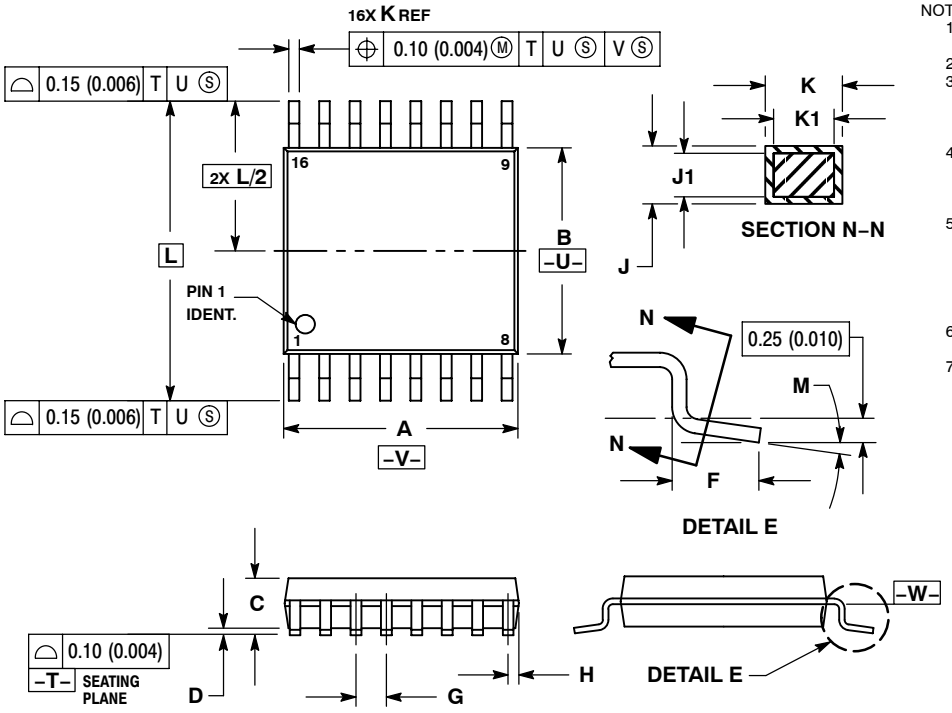
### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

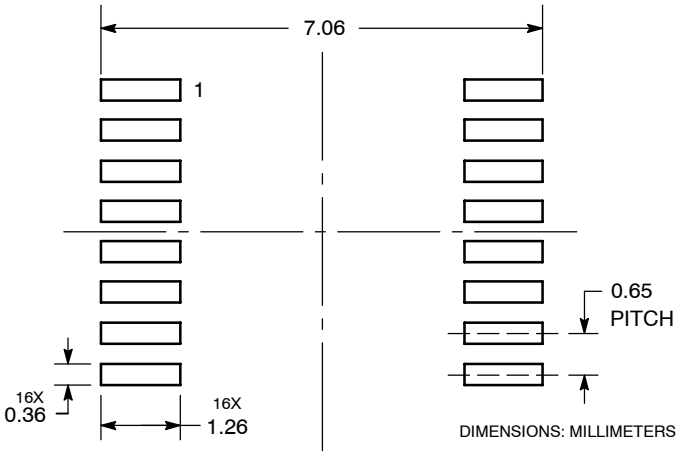
**TSSOP−16**
CASE 948F−01
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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